**BCD TO DECIMAL:**

module BCD\_TO\_DEC(a,b,c,d,y0,y1,y2,y3,y4,y5,y6,y7,y8,y9);

input a,b,c,d;

output y0,y1,y2,y3,y4,y5,y6,y7,y8,y9;

wire w1,w2,w3,w4;

not(w1,a);

not(w2,b);

not(w3,c);

not(w4,d);

and(y0,w4,w3,w2,w1);

and(y1,w4,w3,w2,a);

and(y2,w4,w3,b,w1);

and(y3,w4,w3,b,a);

and(y4,w4,c,w2,w1);

and(y5,w4,c,w2,a);

and(y6,w4,c,b,w1);

and(y7,w4,c,b,a);

and(y8,d,w3,w2,w1);

and(y9,d,w3,w2,a);

endmodule

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|  | | | |
| **Project File:** | ex2.xise | **Parser Errors:** | No Errors |
| **Module Name:** | BCD\_TO\_DEC | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc3s400-4ft256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | No Warnings |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://vk/ex2/BCD_TO_DEC.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** |  |
| **Environment:** | [System Settings](D://vk/ex2/BCD_TO_DEC_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://vk/ex2/BCD_TO_DEC.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of 4 input LUTs | 10 | 7,168 | 1% |  | |
| Number of occupied Slices | 5 | 3,584 | 1% |  | |
| Number of Slices containing only related logic | 5 | 5 | 100% |  | |
| Number of Slices containing unrelated logic | 0 | 5 | 0% |  | |
| Total Number of 4 input LUTs | 10 | 7,168 | 1% |  | |
| Number of bonded [IOBs](D://vk/ex2/BCD_TO_DEC_map.xrpt?&DataKey=IOBProperties) | 14 | 173 | 8% |  | |
| Average Fanout of Non-Clock Nets | 3.57 |  |  |  | |

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| **Performance Summary** | | | | [**[-]**](?&ExpandedTable=PerformanceSummary) |
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | [Pinout Report](D://vk/ex2/BCD_TO_DEC_par.xrpt?&DataKey=PinoutData) | |
| **Routing Results:** | [All Signals Completely Routed](D://vk/ex2/BCD_TO_DEC.unroutes) | **Clock Data:** | [Clock Report](D://vk/ex2/BCD_TO_DEC_par.xrpt?&DataKey=ClocksData) | |
| **Timing Constraints:** |  |  |  | |

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| **Detailed Reports** | | | | | | [**[-]**](?&ExpandedTable=DetailedReports) |
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** | |
| [Synthesis Report](D://vk/ex2/BCD_TO_DEC.syr) | Current | Tue 29. Jul 15:48:00 2025 | 0 | 0 | 0 | |
| [Translation Report](D://vk/ex2/BCD_TO_DEC.bld) | Current | Tue 29. Jul 15:50:17 2025 | 0 | 0 | 0 | |
| [Map Report](D://vk/ex2/BCD_TO_DEC_map.mrp) | Current | Tue 29. Jul 15:50:20 2025 | 0 | 0 | [2 Infos (2 new)](D://vk/ex2/_xmsgs/map.xmsgs?&DataKey=Info) | |
| [Place and Route Report](D://vk/ex2/BCD_TO_DEC.par) | Current | Tue 29. Jul 15:50:24 2025 | 0 | 0 | [2 Infos (2 new)](D://vk/ex2/_xmsgs/par.xmsgs?&DataKey=Info) | |
| Power Report |  |  |  |  |  | |
| [Post-PAR Static Timing Report](D://vk/ex2/BCD_TO_DEC.twr) | Current | Tue 29. Jul 15:50:26 2025 | 0 | 0 | [6 Infos (6 new)](D://vk/ex2/_xmsgs/trce.xmsgs?&DataKey=Info) | |
| [Bitgen Report](D://vk/ex2/BCD_TO_DEC.bgn) | Current | Tue 29. Jul 15:50:30 2025 | 0 | 0 | [1 Info (1 new)](D://vk/ex2/_xmsgs/bitgen.xmsgs?&DataKey=Info) | |

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| **Secondary Reports** | | | [**[-]**](?&ExpandedTable=SecondaryReports) |
| **Report Name** | **Status** | **Generated** | |
| [WebTalk Report](D://vk/ex2/usage_statistics_webtalk.html) | Current | Tue 29. Jul 15:50:30 2025 | |
| [WebTalk Log File](D://vk/ex2/webtalk.log) | Current | Tue 29. Jul 15:50:31 2025 | |

**Date Generated:** 07/29/2025 - 15:50:32

